**Amendments to the Specification:**

Amend the Specification at pages 3 - 4 by replacing the paragraph beginning at page 3, line 28 with the following amended paragraph:

Fig. 5b illustrates one method the short locator tool uses for determining the shortest electrical path for the short 25. Initially, the short locator tool examines the schematic of the circuit 15 (step 40). The locator tool evaluates the connectivity text file of the schematic as shown in Fig. 3b. From the text file, the locator tool knows what the SET and GND ports should be connected to. In this instance, all the SET ports should be connected to CK1 and all the GND ports should be connected to GND1. The locator tool then makes a copy of the artwork shown in Fig. 3c (step 45). The short locator tool does not use the original artwork because the locator tool may be adding a large number of labels which may make the original artwork more difficult for a designer to understand and maintain. Now that a copy of the artwork has been made and the locator tool has examined the text file, the tool knows that all SET ports are ~~suppose~~ supposed to be connected to CK1 and all GND ports are ~~suppose~~ supposed to be connected to GND1. The locator tool will now infer and rename CK1 label for all SET labels and GND1 label for all GND label (step 50). Once all the labels have been inferred, as shown in Fig. 6, the short locator tool invokes the connectivity extract tool. The connectivity extract tool is run again on the copy of the artwork with the inferred labels (step 55). Once the connectivity extract tool is run, the extract tool locates the shortest electrical path between two conflicting labels (step 60).